

IN THE CLAIMS:

Please amend claims 1-3, 5-7, and 11-13 as follows. Please add new claim 15 as follows.

1. (Currently Amended) A method ~~of performing a data transfer between a memory of a processor device and a circuitry connected to said processor device, said method comprising the steps of:~~

performing a data transfer between a memory of a processor device and a circuitry connected to said processor device, wherein said performing comprises

a) setting up at said circuitry a direct memory access (DMA) for transferring data ~~at said circuitry;~~

b) triggering at said circuitry a direct memory access ~~DMA~~ transfer of said data to said processor device;

e) adding in said circuitry said direct memory access ~~DMA~~ transfer to a transaction log;

d) providing said transaction log from said circuitry to said processor device, when said transaction log has reached a predetermined ~~depth~~ limit; and

e) informing said processor device of the availability of said transaction log.

2. (Currently Amended) A method according to claim 1, wherein said triggering and said adding steps b) and e) are repeated until said ~~depth~~ limit has been reached.

3. (Currently Amended) A method according to claim 1, wherein said informing ~~step~~ is performed by initiating an interrupt operation.

4. (Original) A method according to claim 3, wherein said interrupt operation initiates an interrupt service routine.

5. (Currently Amended) A method according to claim 1, further comprising the ~~step of~~ validating said transferred data at said processor device based on said available transaction log.

6. (Currently Amended) A method according to claim 1, wherein said circuitry is an application specific integrated circuit ASIC.

7. (Currently Amended) A method according to claim 1, further comprising the ~~step of~~ storing said transaction log in said memory.

8. (Withdrawn) A processor device having a memory which can be accessed by a connected circuitry, said processor device being arranged to validate data, transferred to said memory by a direct memory access, based on a transaction log provided to said processor device.

9. (Withdrawn) A processor device according to claim 8, wherein said processor device is arranged to validate said transferred data in response to an interrupt triggered by said connected circuitry.

10. (Withdrawn) A processor device according to claim 8, wherein said processor device is a digital signal processor.

11. (Currently Amended) An integrated circuit comprising: having
means for providing functionality configured to provide access to a processor device, wherein said integrated circuit is configured ~~being arranged~~ to set up a direct memory access (~~DMA~~) for transferring data via said access means, to trigger a direct memory access ~~DMA~~ transfer of said data, to add said direct memory access ~~DMA~~ transfer to said transaction log, to provide said transaction log to said processor device

when said transaction log has reached a predetermined ~~depth~~ limit, and to issue an information indicating the availability of said transaction log.

12. (Currently Amended) A ~~An~~ integrated circuit according to claim 11, wherein said integrated circuit is ~~arranged~~ configured to issue said information by triggering an interrupt.

13. (Currently Amended) An integrated circuit according to claim 11, wherein said integrated circuit is an application specific integrated circuit ASIC.

14. (Withdrawn) A system for performing a data transfer between a memory of a processor device and a circuitry connected to said processor device,

a) wherein said circuitry is arranged to set up a direct memory access (DMA) for transferring data, to trigger a DMA transfer of said data to said processor device, to add said DMA transfer to a transaction log, to provide said transaction log to said processor device when said transaction log has reached a predetermined depth limit, and to inform said processor device of the availability of said transaction log; and

b) wherein said processor device is arranged to validate said transferred data based on said provided transaction log.

15. (New) An integrated circuit comprising:

performing means for performing a data transfer between a memory of a processor device and a circuitry connected to said processor device;

setting means for setting up a direct memory access for transferring data at said circuitry;

triggering means for triggering a direct memory access transfer of said data to said processor device;

adding means for adding said direct memory access transfer to a transaction log;

providing means for providing said transaction log to said processor device, when said transaction log has reached a predetermined limit; and

informing means for informing said processor device of the availability of said transaction log.